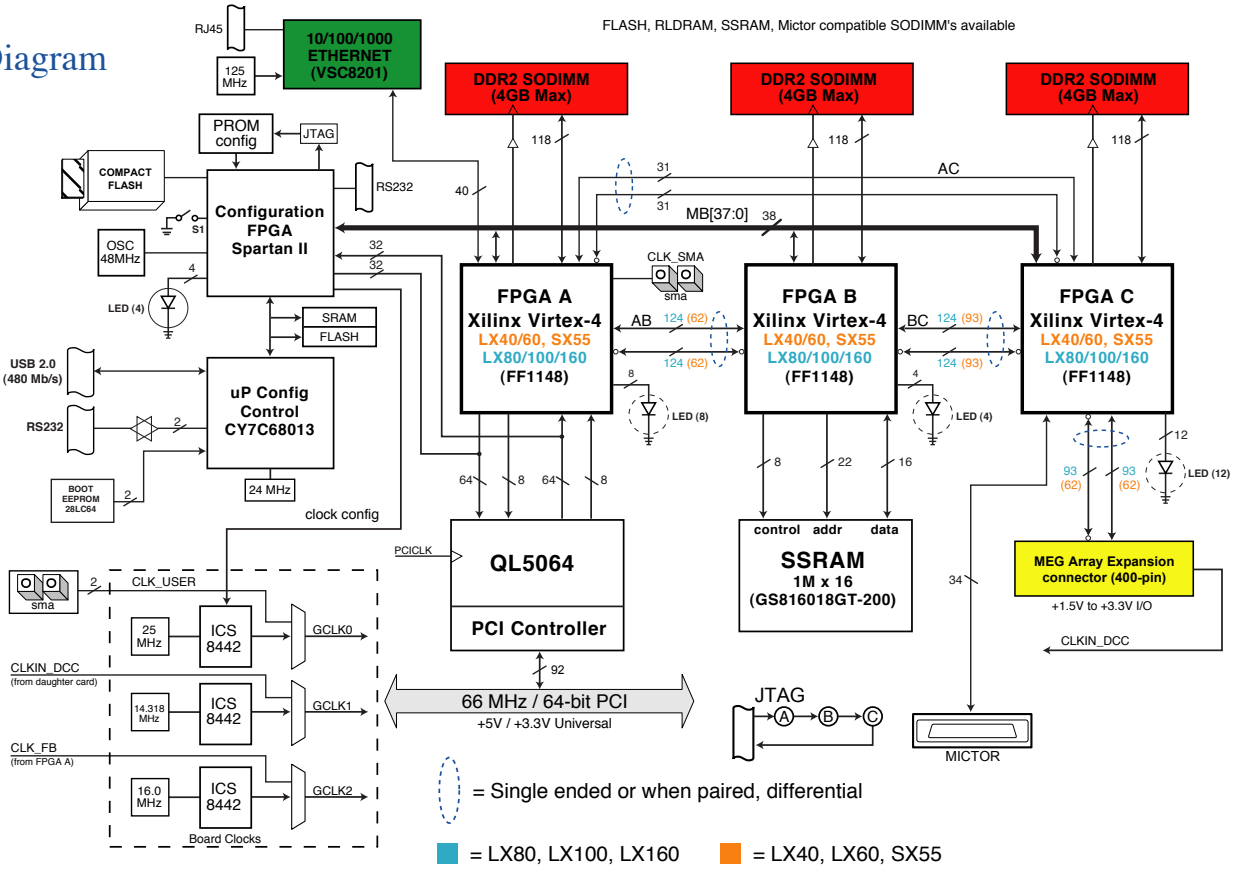
Product Brief
April 2006
Ver. 1.1

DN8000K10PSX
Virtex-4 based ASIC Prototyping Engine

Features

- PCI hosted logic prototyping system available with Xilinx Virtex-4 FPGA's.
- Stuffing options for 1,2, or 3 FPGA's from the following list:
  - 'LX' family: LX40, LX60, LX80, LX100, LX160
  - 'SX' family: SX55
  - -10, -11, -12 speed grades
- 100% FPGA resources available for user application
- Nearly 3.4M ASIC gates (LSI measure) with 3 LX160's
  - 1536, 18x18 multipliers with 3 SX55's
- All FPGA to FPGA interconnect is pair-matched LVDS differential
  - 350Mhz differential chip to chip
  - 200Mhz single-ended (with I/O FF)
  - Reference designs for integrated ISERDES/OSERDES
  - 10x pin multiplexing per LVDS pair
- Synplicity Certify™ models for partitioning assistance
- 10/100/1000BASE-T Phy connected to FPGA A
  - Vitesse VSC8201
  - Standard RJ45 connector
- 3 separate programmable clock synthesizers for global clocks (ICS8442)
  - GCLK[2:0]
  - User configurable via Compact FLASH, PCI, or USB
- Dedicated 64-bit/66MHz PCI Bridge - QL5064
  - No FPGA resources consumed for PCI
  - Maximum PCI data transfer rate: 533mb/s
  - Programmable Target Prefetching/Write Posting
  - PCI2.2 Compliant
  - Zero Wait State Master and Target Bursting
  - Five Independent Master DMA Channels:
    - 2 Transmit, 2 Receive, 1 Single PCI Access (SPCI)
    - DMA Chaining/Scatter Gather
  - Mailboxes, Interrupts
- Advanced FPGA configuration via PCI, USB2.0 or Compact FLASH
- Partial reconfiguration support on all FPGAs
- 3 separate DDR2 SODIMMs (200MHz), one for each FPGA
  - 64-bit data width, 200MHz operation
  - PC2-3200/PC2-4200
  - Addressing and power to support 4GB in each socket
  - Verilog/VHDL reference design provided (no charge)
  - DDR2 SODIMM data transfer rate: 25.6Gb/s
  - Alternate pin-compatible SODIMMs:
    - QDR SSRAM, FLASH, SSRAM, RLDRAM, Mictor
- RS232 port for embedded uP observation/debug
  - Multiplexed via SpartanII FPGA
  - Accessible from any FPGA
- Enough Status LED's to blind a small ferret
- Standalone operation with off-the-shelf ATX power supply.
- One, 400-pin MEG-Array Expansion Connector for custom daughter cards
  - 93 pairs LVDS (or 186 single-ended)
  - I/O voltage controlled by daughter card (+1.5V -> +3.3V)
  - DNMEG_Obs Observation Daughter Card
- Full support for embedded logic analyzers via JTAG interface
  - ChipScope, ChipScope PRO
  - Identify™ from Synplicity

Block Diagram



Description

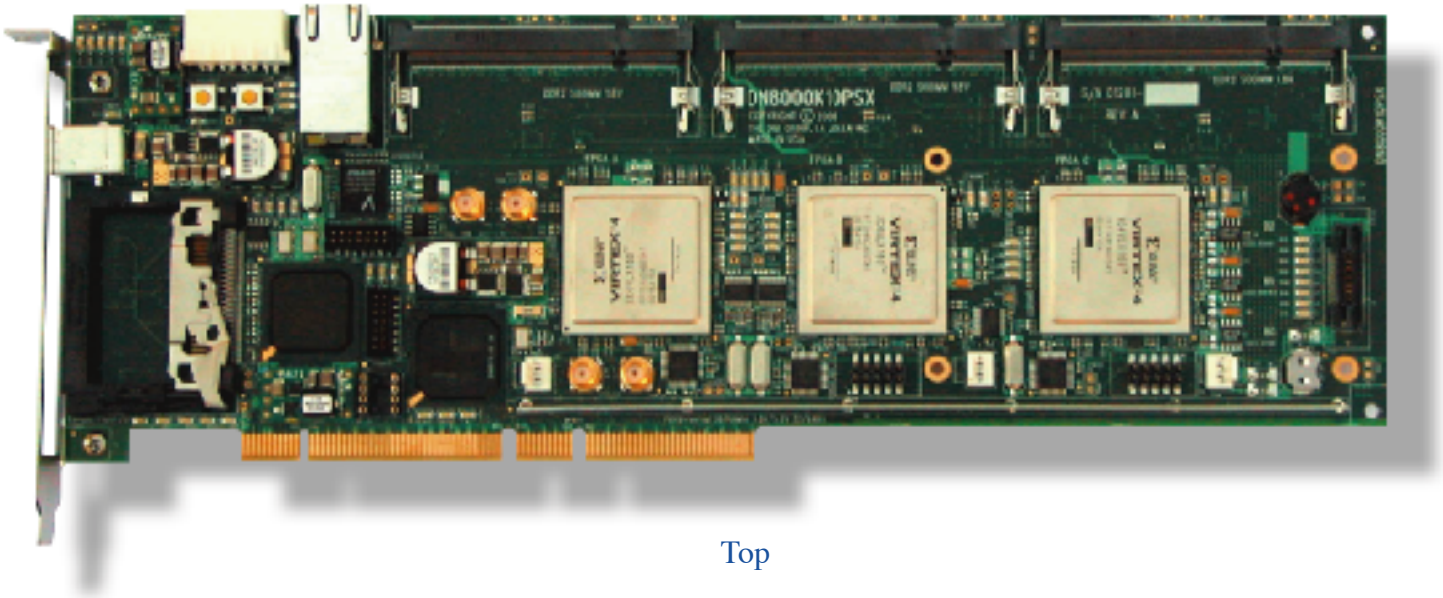
The DN8000K10PSX is a complete logic emulation system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. The DN8000K10PSX is hosted in a 32-bit or 64-bit PCI slot (33/66MHz) or can be used stand-alone. A single DN8000K10PSX configured with 3 4VLX160's can emulate up to 3.4 million gates of logic as measured by LSI. This product can also be stuffed with the SX55, which supports 512-18x18 multipliers per FPGA enabling high performance DSP applications. Any FPGA position can be stuffed with an FPGA of any speed grade from the following list: LX40, LX60, LX80, LX100, LX160, SX55.

The DN8000K10PSX achieves high gate density and allows for fast target clock frequencies by utilizing FPGA's from Xilinx's Virtex-4 LX/SX families for logic and memory. High I/O-count, 1148-pin, flip-chip BGA packages are employed, providing for abundant, fixed interconnect between the FPGA's. All FPGA interconnect is single-ended or differential, with LVDS clocked at 350MHz+. In addition, the OSERDES/ISERDES functionality is thoroughly tested and characterized, allowing for 10x DDR pin multiplying on differential pairs between FPGA's and dramatically easing the partitioning problem. The industry's highest performance PCI Bridge, the QL5064, enables data transfer via master-moding and chaining, without making any resource demands on the Virtex-4 FPGA's. Three DDR2 SDRAM SODIMM's are provided, one per FPGA, allowing for up to 12GB of DDR2 memory. Optional socket-compatible SODIMM's are available: QDR SSRAM, FLASH, SSRAM, RLDRAM, and Mictor. Each socket is tested at 200MHz, and reference designs are provided.

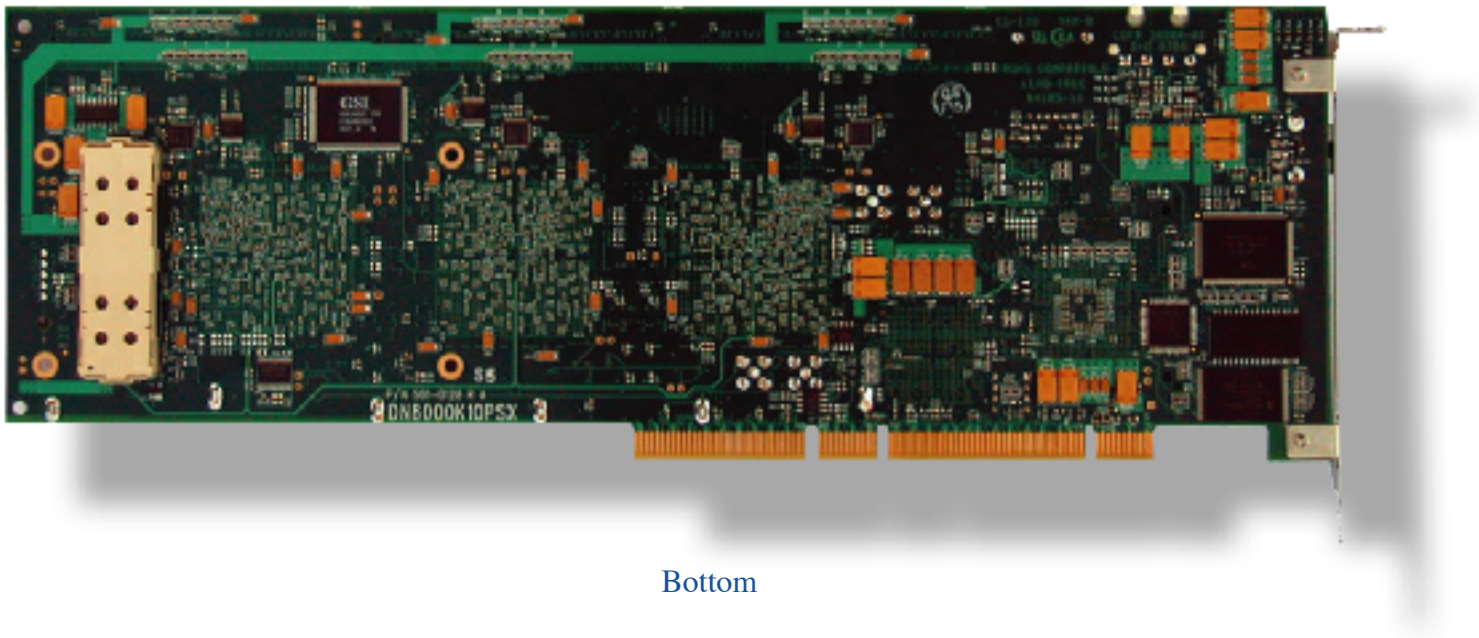
Gigabit Ethernet connectivity is provided via a Vitesse VSC8201 physical layer transceiver. With the appropriate MAC in FPGA A, the DN8000k10PSX can interface to 10BASE-T, 100BASE-T, and/or 1000BASE-T. An MII interface is used to connect the FPGA to the VSC8201 Phy.

A total of 93 LVDS pairs of FPGA pins (186 single-ended) are provided on the bottom of the PWB via a single 400-pin MEG-Array expansion connector and interfaces to FPGA C. This expansion header can be used for logic analyzer-based debugging or for pattern generator stimulus by utilizing the **DNMEG_Obs** Observation Daughter card. Custom daughter cards can be mounted to this connector as a means to interface the DN8000k10PSX to application-specific circuits. Reference material such as DDR2 SDRAM controllers and PowerPC code is included (in Verilog, VHDL, C) at no additional cost.

FPGA	Speed Grades (slowest to fastest)	Slices or LE's	FF's	Gate Estimate		Max I/O's	FF's in IO pad	Multipliers (18x18)	PowerPC Blocks	Memory		
				Max (100% util)* (1000's)	Practical (60% util)* (1000's)					Blocks (18kbits)	Total (kbits)	Total (kbytes)
SX55	-10,-11,-12	24,576	49,152	690	410	640	10	512	0	320	5,760	720
LX40	-10,-11,-12	18,432	36,864	520	310	640	10	64	0	96	1,728	216
LX60	-10,-11,-12	26,624	53,248	750	450	640	10	64	0	160	2,880	360
LX80	-10,-11,-12	35,840	71,680	1,000	600	768	10	80	0	200	3,600	450
LX100	-10,-11,-12	49,152	98,304	1,380	830	768	10	96	0	240	4,320	540
LX160	-10,-11,-12	67,584	135,168	1,890	1,130	768	10	96	0	288	5,184	648



Top



Bottom

For technical applications and sales support, call 858.454.3419

1010 Pearl Street, Suite #6
La Jolla, CA 92037-5165
Phone: 858.454.3419
Fax: 858.454.1728
E-Mail: sales@dinigroup.com
Web: http://www.dinigroup.com