Product Brief
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# DN_DPB_S327

***Monster's Mailman***

## Cyclone III FPGA Algorithmic Acceleration Peripheral
### For High Performance Computing
**Featuring 27 Altera Cyclone III FPGAs**
**Hosted via 10/100 base-T Ethernet**

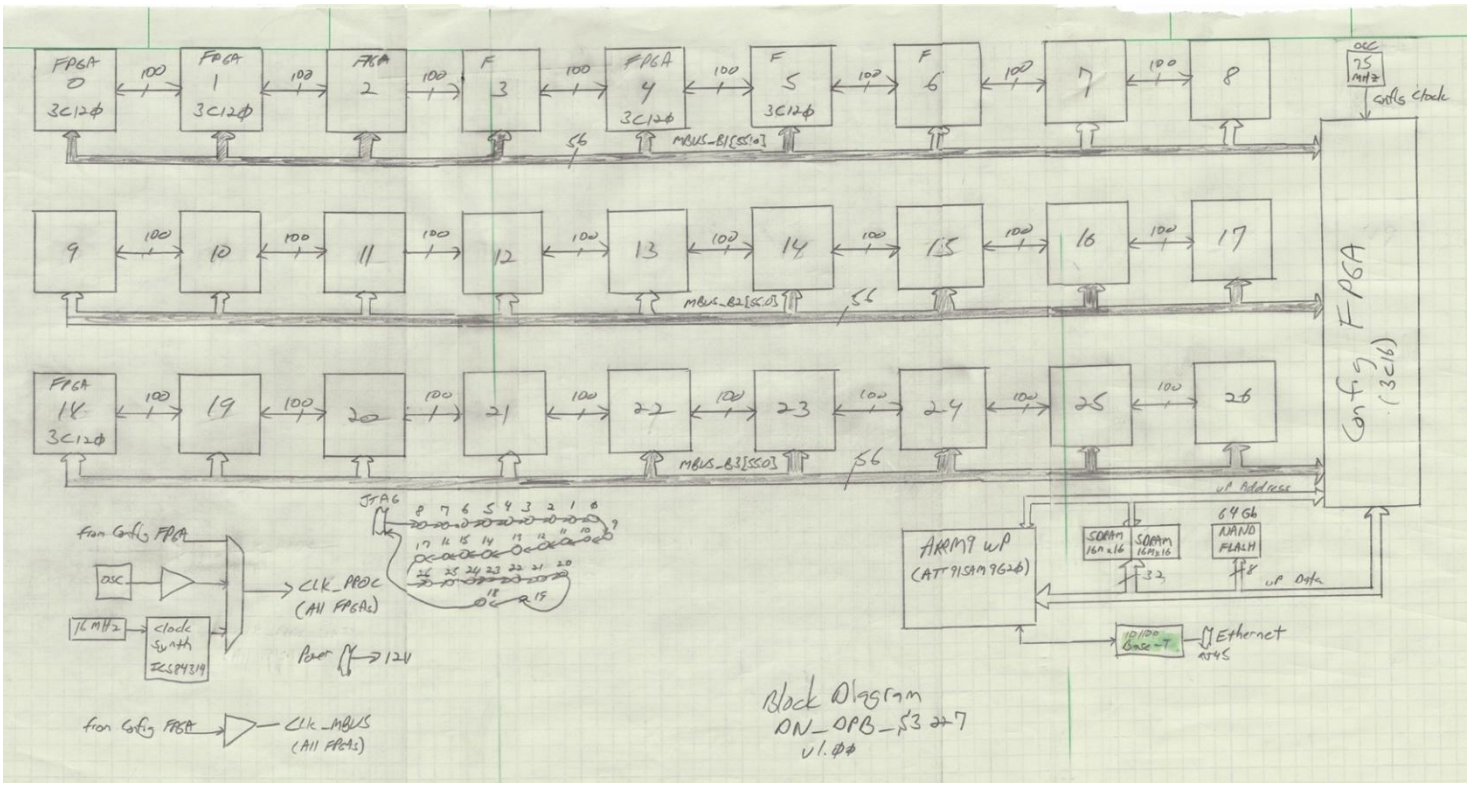
## Features

- 27, EP3S120 Altera Cyclone III FPGAs (FF484)
  - 100% dedicated to the user application
  - Each FPGA contains:
    - 119,000, 4-input LUT/FF pairs
    - 486 kbytes of memory
    - 432 – 18x18 multipliers
    - ~1million ASIC gates of logic
  - Organized as three rows of 9 FPGAs
- FPGAs can be configured identically or individually
- Hosted via 10/100/BASE-T Ethernet or stand alone
- FPGA to FPGA interconnect:
  - Nearest horizontal connections: 100 single-ended
  - Three 56-bit busses – 1 for each horizontal set of 9 FPGAs
- Atmel AT91 ARM Thumb Microcontroller (ARM9)
  - ARM926EJ-S processor
    - 400MHz CPU frequency
    - 32-KByte Data Cache
    - 32-KByte Instruction Cache, Write Buffer
    - Memory Management Unit
  - 64 MB of external SDRAM
    - Organized as 16M x32
  - 64 Gb of external NAND FLASH
  - Gigabit Ethernet interface
    - 10/100/ GbE (RJ45 connector)
  - After FPGA configuration, CPU dedicated entirely to user application
  - LINUX operating system
    - Source and examples provided via GPL license (no charge)
  - RS232 port for terminal interface

- Two independent, low-skew global clock differential networks
  - CLK_PROC
    - Frequency programmable with range of 31.25MHz to 700 MHz
  - CLK_MBUS
- +12V external supply required for power
- Fast and Painless FPGA configuration via Ethernet
- Full support for embedded logic analyzers via JTAG interface
  - SignalTap™ and other third-party debug solutions

| | FPGA | Speed Grades (slowest to fastest) | LUT Size | FF's | Gate Estimate | | Multipliers (18x18) | Memory | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Max (100% util) (1000's) | Practical (60% util) (1000's) | | MLAB (640) | M9K (9 kbit) | M144K (144 kbit) | Total (kbits) | Total (kbytes) |
| Cyclone III | 3C16 | -8,-7,-6 | 4-input | 15,408 | 216 | 134 | 56 | 0 | 56 | 0 | 504 | 63 |
| | 3C120 | -8,-7 | 4-input | 119,088 | 1,667 | 1,000 | 288 | 0 | 432 | 0 | 3,888 | 486 |

# Description




## *Overview*

Designed for high performance computing applications, the **DN_DPB_S327** is an FPGA-based peripheral that allows algorithm developers to employ hardware-in-the-loop acceleration utilizing a large grid of 27 cost effective, Altera Cyclone III FPGAs. Data movement to/from the FPGA grid is accomplished via 10/100 base-T Ethernet. We have several chassis configurations that can fit up to 20 of these cards in a single 19" rack. Contact the factory for details.

## The FPGAs: 27 Altera Cyclone III

The 3C120 from Altera's Cyclone III family is utilized and this is the second largest member of this cost effective (read: **CHEAP**) family. The Cyclone III FPGA family has an impressive price/performance ratio for hardware-in-the-loop accelerators, with device power consumption much lower than the higher performance FPGA families.

Features of Cyclone III include an efficient, 4-input look-up table (LUT) logic, 9 Kb (2 x 9 Kb) block RAMs, along with 18 x 18 multipliers. We use the FF484 package, which gives us the highest possible circuit board density. 100% of the FPGA resources are dedicated to your application. The 27 FPGAs have the identical pinouts and can be configured with the same file, eliminating the time consuming task of optimizing the same design for 27 different pinouts. The FPGAs can be configured with different functionality and programmed separately.

FPGA configuration files can be stored on the board in a 64Gb NAND FLASH, but the most likely usage model is to have the host system store and orchestrate FPGA configuration.

We do not supply simulation, FPGA synthesis, or place/route. But expensive, third-party synthesis tools are not needed and no longer required to get good quality of results. In truth, the cost effective Quartus®II tools available directly from Altera have proven in benchmarks to be superior to the expensive third party tools.

## An on board ARM9 processor

An AT91SAM9G20 AT91 ARM Thumb microcontroller runs an ARM9 processor at 400MHz. This processor boots to LINUX. Source and 'C' examples under a GPL license are provided. 100% of the processing power of this microcontroller is dedicated to your application. 64 megabytes (16M x 32) of external SDRAM is stuffed standard, along with a 64 Gb NAND FLASH. Processor code can reside in the NAND FLASH at boot, or downloaded via Ethernet. Data movement to/from the 27 Cyclone III FPGAs is aided by a *Config FPGA* (Cyclone II 3C16).

## Debug

A JTAG connector provides an interface to SignalTap and other third party debug tools.