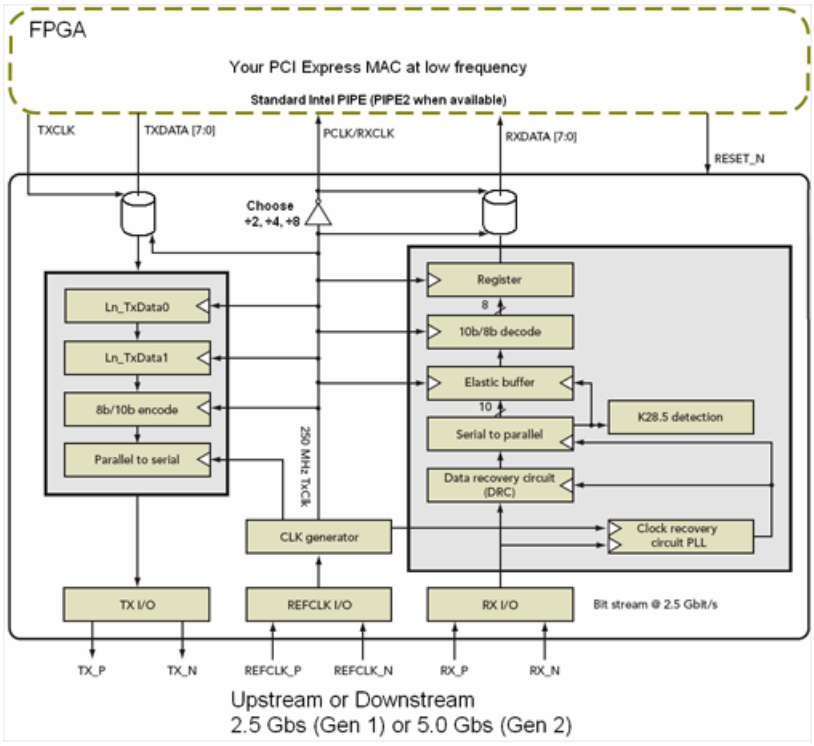
High Speed Prototyping for PCIe Designs

ASIC Prototyping with FPGAs on the PCIe bus requires slowing down the PIPE

ASIC developers who wish to emulate the PCIe bus in their designs face some challenges. Of course they want to validate IP (often purchased from a vendor) that has never been tested in their exact application. The prudent developer will insist on high speed prototyping to prove their designs performance, but most PCIe ASIC designs will not run in FPGAs at full speed.

The clocks in PCIe systems are related the the data rate of 2.5 Gbits/s and cannot be throttled. Therefore PIPE (PHY to MAC) interfaces in FPGA Prototypes are required to run at 125/250 MHz for GEN 1 and 250/500MHz for GEN 2. This is too fast for most FPGA emulations to operate so the developers of PCIe ASICs were out of luck. Until now. The Dini Group has developed a Slowdown Core that enables IP interfacing to the standard Intel PIPE at a much lower frequency. The Dini Group IP block enables frequency division by a factor of 2, up to a maximum of 8. Users can run their designs at 31.25 to 125MHz and still maintain full PCIe functionality and verify their system with off-the-shelf motherboards.



When connected between the user's design and the PCIe serial interface the Slowdown Core allows comfortable FPGA clock frequencies with 8 or 16-bit standard Intel PIPE interface. There is support for 1,4, and 8-lane configurations. No user MAC interface modifications are required, and developers now have a high speed method for complete design verification.

The PIPE Slowdown Core is available with all Dini Group PCIe boards.

PCIe prototyping challenges also include some not so obvious hardware problems. In designs that are large enough to require multiple FPGAs the circuit board itself is a major problem. Only the largest V5 (V6 when available) devices make any sense: the less partitioning, the better. If the board is to plug into a standard PCIe edge connector, then thickness limits the designers ability to manage all the interconnects. This is a major hurdle when routing 1760 pin BGA chips. At the Dini Group we have been solving these kind of problems for many years, we offer "plug-in" boards with up to 32 million ASIC gates.

PCIe ASIC Prototyping Boards from the Dini Group are available with 2 to 16 Xilinx V5, LX 330s. For more detail please visit www.dinigroup.com where you will find lots of clever solutions for the challenges of ASIC Prototyping.