

PCIe PIPE Slowdown Core

Features

- IP block that throttles a PHY Interface to a slower frequency
 - Easier prototyping of PCIe logic
 - Frequency division by a factor 2 to a maximum of 8
 - 250MHz/125MHz -> 31.25MHz
- PCIe GEN1 (2.5 Gb/s) and PCIe GEN2 (5.0 Gb/s)
- 1, 4, or 8-lanes
 - 8-bit or 16-bit per lane
- Signal Interface identical to the Intel PIPE specification
 - PHY Interface for the PCI Express Architecture (Version 2.00)
 - No user MAC interface modifications required
- Support for power management and power state transition
 - L0, L0s, L1, L2, L3
 - Beacon signaling (L2 -> L0)
 - Receiver detection
- Simulation models and example interface code provided

Description

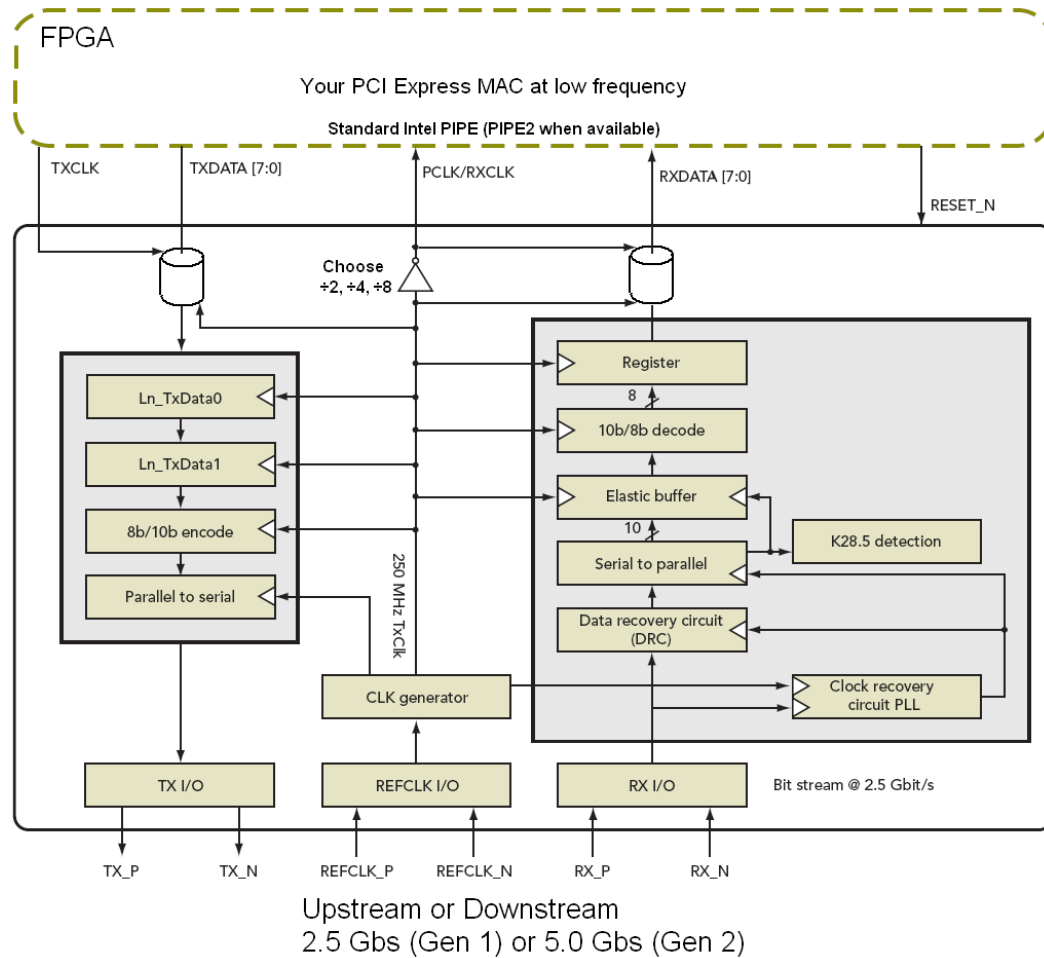
The process of prototyping PCIe systems with FPGA's is easier if the frequency is reduced to a number comfortably within an FPGA's capability. This is troublesome in PCI Express systems since the clocks are generated using high performance PLL's and cannot be readily throttled. So PIPE interfaces in FPGA prototypes are required to run at 125MHz/250MHz for GEN1 PCIe and at 250MHz/500MHz for GEN2 and this is too fast. The DINI Group PCIe PIPE Slowdown Core enables IP interfacing to the standard Intel PIPE at a much slower frequency.

Connecting the Slowdown Core between the user's design and the PCIe serial interface allows the user to build a design that runs at 31.25 – 125 MHz, instead of the full speed of 250 MHz (or 500MHz), and still maintain full PCIe functionality. The Slowdown Core can be configured with an 8-bit or 16-bit PIPE interface, and has support for 1, 4, and 8-lane configurations.

The Slowdown Core will automatically handle polarity inversion and allows the user to enable or disable: 1) the generation and filtering of skip-ordered sets, 2) byte-alignment across the active lanes of the PIPE interface, and 3) LFSR scrambling.

The DINI Group PCIe Slowdown Core is only available in DINI Group PCIe boards, and licensing is done via an encryption key that is programmed at the factory.

Source code is provided for the Slowdown User I/O module to interface to the Slowdown Core.



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