



PCI Express Cores

(Endpoint, Root port, Dual RP/EP, Switch port)

Company

- PCI Express - FOCUS
- Total PCI Express Solutions - IP, Design Services - Integration through Silicon
- Domain Expertise - PCI/PCI-X, PC Architecture, Power Management, Storage, Networking
- Solutions engineered by SoC/ASIC/FPGA industry veterans
- Located in Silicon Valley, USA.

Overview of IP Cores for PCI Express

ASIC Architect's high performance cores come in multiple Datapath flavors with the choice of single or dual PIPE PHY Interface. The cores have been architected to achieve very low latency, high throughputs, and quick timing closure with low small silicon footprint. The user interface provides practical and integration-friendly mechanisms for the integration of the cores to user logic. Please refer to the product matrix below to choose the core for your ASIC/FPGA.

PCI Express Cores	x8	x4	x2	x1	x16
Endpoint	64 bit 128 bit	32 bit 64 bit 128 bit	32 bit 64 bit 128 bit	32 bit 64 bit 128 bit	128 bit
Root Port	64 bit 128 bit	32 bit 64 bit 128 bit	32 bit 64 bit 128 bit	32 bit 64 bit 128 bit	128 bit
Dual Mode (EP/RC)	64 bit 128 bit	32 bit 64 bit 128 bit	32 bit 64 bit 128 bit	32 bit 64 bit 128 bit	128 bit
Switch Port (Upstream Downstream)	64 bit 128 bit	32 bit 64 bit 128 bit	32 bit 64 bit 128 bit	32 bit 64 bit 128 bit	128 bit

ASIC Architect, Inc.
1850 Warburton Ave, Suite#104
Santa Clara CA 95050

(408) 247 - 9931
sales@asic-architectinc.com
www.asic-architectinc.com



PCI Express Cores

(Endpoint, Root port, Dual RP/EP, Switch port)

Architecture

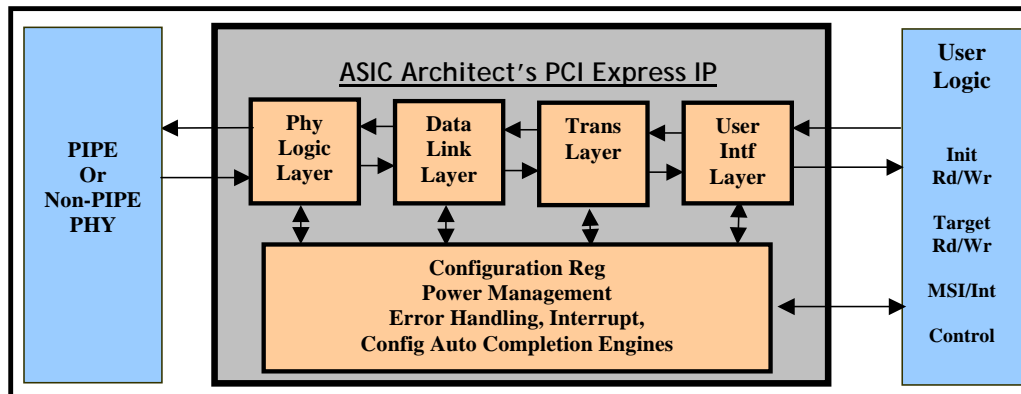
- Architect-ed by industry veterans with SoC Expertise
- Scalable
- Pipelined
- Plug-and-Play User Interface
- Easy to Verify
- Ease of DFT and DFD

Design

- Technology Independent Design for ASIC and FPGA
- Synchronous Design
- Proven Methodology for IP Reuse
- We discover tricky and boundary conditions before they discover us

Reliability

- Silicon-proven
- PCI-SIG Integrators List
- Verified with multiple 3rd party test-suites for PCI Express





PCI Express Cores

(Endpoint, Root port, Dual RP/EP, Switch port)

Features:

- PCI-SIG's PCI Express Spec. 1.0a and 1.1 Compliant
- **High Performance**
 - Supports upto 8 Virtual Channels (VC0...VC7)
 - Isochronous Traffic Support
 - Multiple Pipelined Memory Read Capability
 - Pipelined/Streaming Operation for Memory Write Requests
 - Low Transmit Latency Core
 - Low Receive Latency Core
 - Low Silicon Footprint
 - Non-blocking Architecture
 - Maximum PCI Express Link Utilization
 - Complete Power Management Support
 - Multifunction Endpoints
- **Plug and Play Type Application Interface**
 - Easy-to-integrate Interface with User logic
 - Streamlined User Interface with reasonable number of interface signals
 - Controllability for critical device parameters
- **Parameterized Core**
 - Parameterized RTL
 - Supports both **cut-through** scheme and **store & forward** scheme for forwarding TX packets
 - Core operate at all allowed speeds down to x1 mode
 - User configurable virtual channels
 - Selectable ECRC and Advanced Error Reporting Support
 - Configurable Type-0 (Endpoint) or Type-1 (RP, Switch) Config headers

ASIC Architect, Inc.
1850 Warburton Ave, Suite#104
Santa Clara CA 95050

(408) 247 - 9931
sales@asic-architectinc.com
www.asic-architectinc.com



PCI Express Cores

(Endpoint, Root port, Dual RP/EP, Switch port)

ASIC Deliverables

- Verilog RTL
- Testbench and Models for Simulation
- Sample Synthesis Script
- Sample Static Timing Analysis Script
- Support from Core Integration through Silicon Bring-up

FPGA Deliverables

- Verilog RTL or Netlist
- Testbench and Models for Simulation
- Sample Synthesis Script
- Sample Static Timing Analysis Script
- Support from Core Integration through Silicon Bring-up